

# A Chipset for a MKII Style Correlator

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**Abstract.** Use of FPGAs allows to develop, even in few samples, medium complex, flexible, and cheap systems. It has been developed a set of chips to test the feasibility building a MKII style correlator for Italian antennas of Istituto di Radioastronomia CNR designed on the basis of “state of the art” components for easy and efficient production and maintenance. This could allow running a small but complete network and extending VLBI usage by ad hoc MKII experiments. It is presented a brief description of each chip and an overall design for such type of correlator. The chipset is designed to work at 4 MHz sample rate, but could potentially work at higher clock rates.

## 1. Introduction

About five years ago Istituto di Radioastronomia CNR of Bologna got a MKII type Block 0 correlator from Caltech. The correlator has been operational for only short periods due to maintenance problems, especially of the control computer. Meanwhile the MKII experiments have been deleted from the official EVN VLBI scheduling being replaced with MKIIIA, VLBA, and MKIV experiments.

Interest in MKII experiments is still effective for the Italian antennas of Medicina and Noto because it represents a very cheap way to perform “ad hoc” experiments using already operational data acquisition terminals. A correlator that is accessible “around the clock” is also a natural element to complete the network of the Italian antennas.

One action has been the trial of the reactivating of the old system but also the possibility to build a new system, more compact and cheap, using advanced technology, has been evaluated.

FPGA devices seem to be the components to meet our specifications of small dimension, low costs in terms of manpower and components, and the use of new technology, in particular the on field reprogrammable type. Costs are not too high even in low quantities and reprogrammability is a very useful characteristic in order to simplify debugging and flexible use of hardware.

In general FPGAs are composed by a matrix of configurable blocks, a group of surrounding I/O blocks and interconnection resources. The internal complexity and the available number of configurable blocks depend on the FPGA family used. Internal configurable blocks may include logic function generators, registers and RAM. I/O blocks are interfaces between the external world and the device and they

also may include registers and simple logic. Complex interconnection resources are used to connect the programmed blocks in order to create the desired configuration. In case of reprogrammable components, the hardware function may be dynamically changed loading different configuration files, possibly by remote control.

Using FPGA technology we developed four chips to test the possibility to realise a MKII correlator. They are:

- correlator and integrator
- fringe rotator
- video decoder
- audio decoder with tape synchronisation.

We will discuss an introduction of the chip design and a possible 5 stations correlator.

## 2. Correlator Chip

Using reprogrammable gate arrays it is possible to download different configurations to the components, which allows to modify the hardware function in an easy way. Modification is performed by loading a particular file. Following this principle we realised three different correlator configurations using almost all logic available in the chip used:

- 8 lags with 22-bit counters and output of 16 most significant bits;
- 16 lags with 12-bit counters and output of 8 most significant bits;
- 32 lags with 6-bits counters and output of 4 most significant bits.

The device used is a 9000 gates equivalent. More than one chip may work together in order to perform as a versatile and powerful system with the possibility to change the architecture remote controlled. Interconnections between chips and signal distribution can be chosen by loading different configuration files.

Figure 1 reports a schematic view of one channel of the two available in the complex correlator chip, multiplication scheme being  $1 \times 1$  bit. The functional parts are the following:

- data input;
- data blanking and 180 degree shift;
- correlation stages with multipliers and integrators;
- clock counter and internal flow logic;
- storage registers;
- output multiplexer.

A chip including only integration stages (8-16-32) may be connected to the correlator chip in order to increase counting capabilities. A correlation section with two chips configured as correlator + correlator or integrator has the following performances:

- 8 lags with 32-bit counters and output of 26 most significant bits;
- 16 lags with 28-bit counters and output of 24 most significant bits;
- 32 lags with 15-bit counters and output of 13 most significant bits;
- 64 lags with 6-bit counters and output of 4 most significant bits.

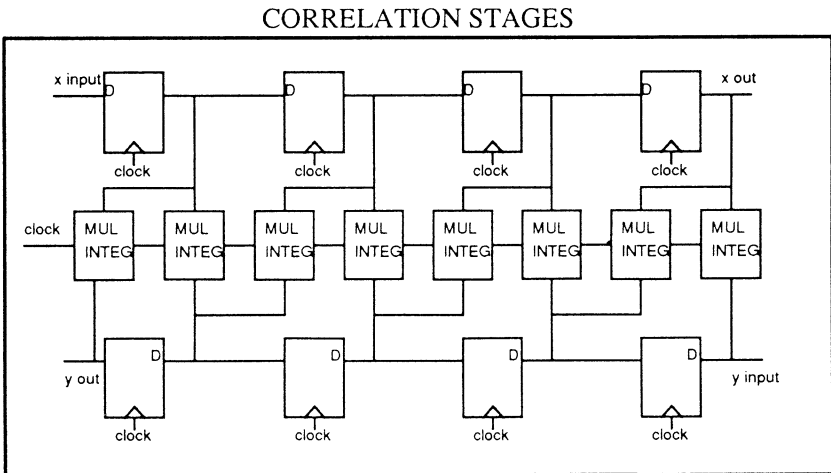
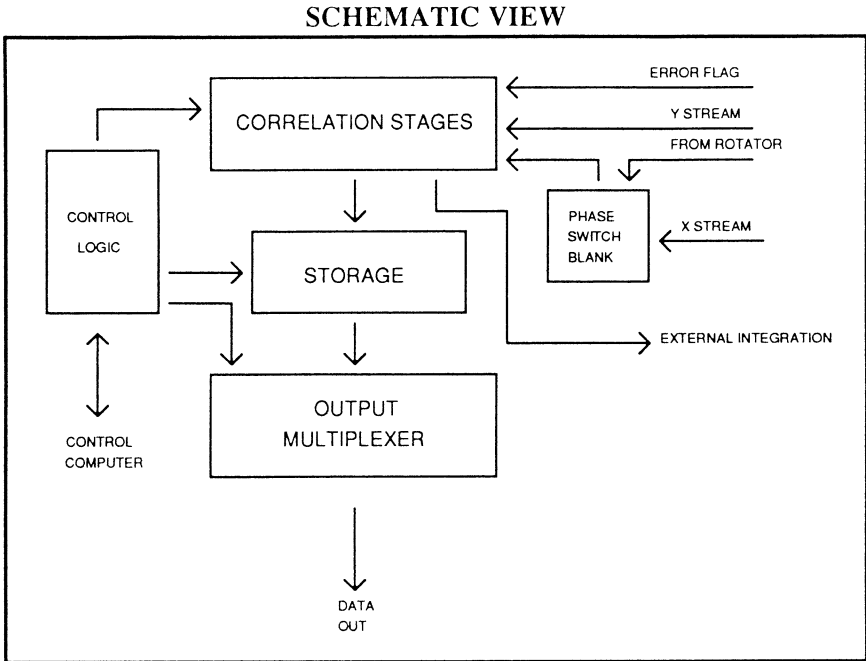


Fig. 1. Schematic view of the correlator chip and data flow organization.

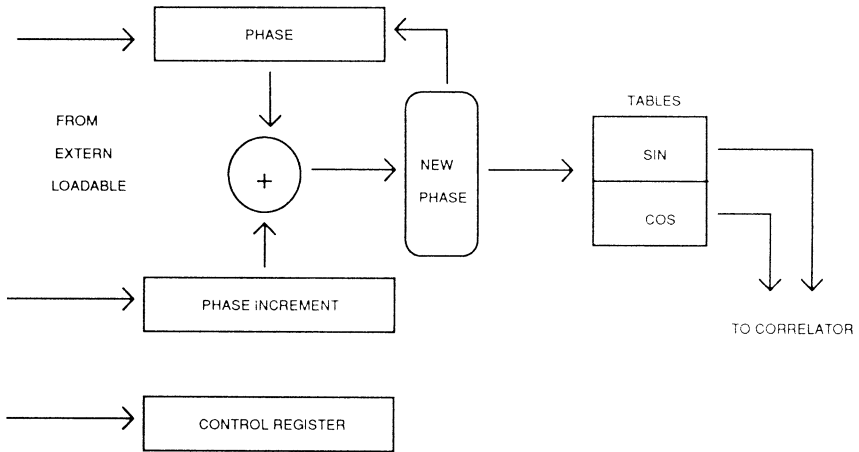


Fig. 2. Schematic view of the rotator chip.

### 3. Fringe Rotator Chip

To stop interference fringes caused by variable interferometer geometry due to earth rotation, the data stream coming from one station is usually multiplied by a digitised three level sin and cos function. Such a function is performed by a circuit called fringe rotator.

The fringe rotator chip has been realised using a component with 3000 gate equivalents. In Fig. 2 a schematic block shows the architecture. There are two 32-bit registers for phase and phase increment. A control logic register allows to select the mode: initial configuration, running configuration. Initially both registers are loaded by external control and then the chip is enabled to run clocked by the system clock. Each clock cycle the phase is summed to phase increment and the result loaded into a summation register. The 4 most significant bits of this register point into a ROM table that represents 16 values of a three level sin and cos function. At 4 MHz sample rate the system is able to produce sin and cos function within a frequency range 1 mHz–250 KHz in steps of 1 mHz.

### 4. Video and Audio Decoder Chips

The video decoder chip is responsible for clock and data extraction of the biphasic signal coming from the recorder, for data check and resynchronization. A 4200 gates equivalent device has been used.

The schematic block in Fig. 3 illustrates the job. The associated clock information from the data obtained is reconstructed and a decoder finds the BOF (beginning of frame) and SYNC words embedded in the data. A counter is used to verify the correct

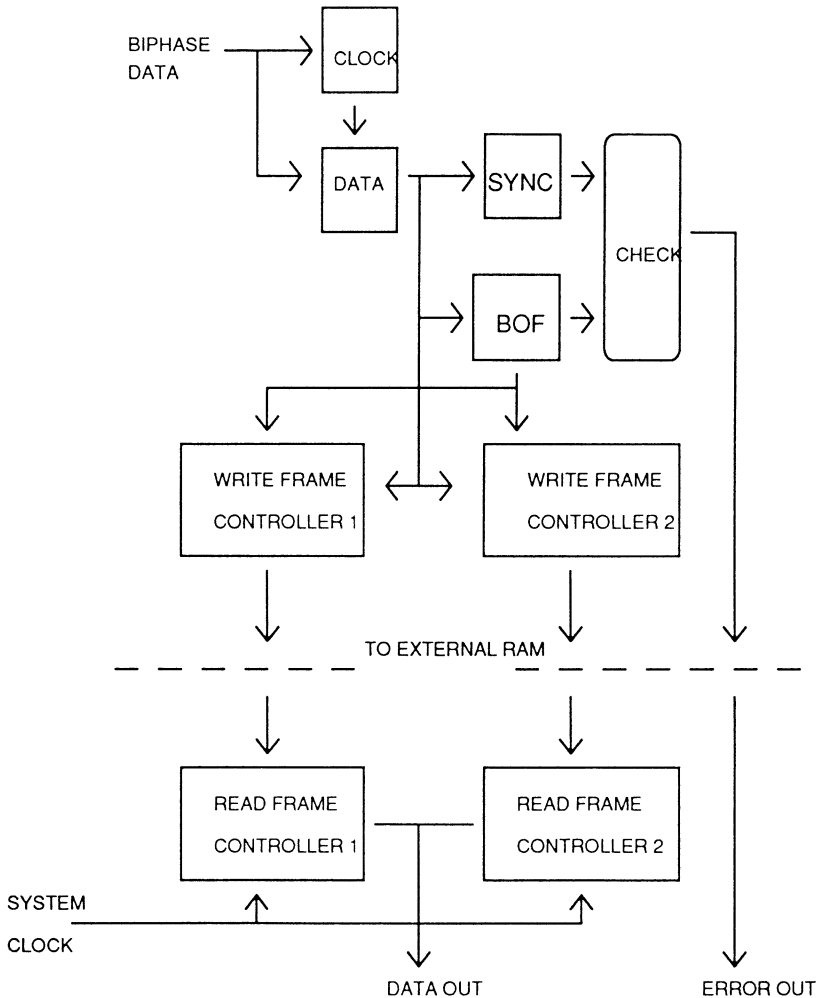


Fig. 3. Schematic view of the video decoder chip.

number of bits between two SYNC words. A status check is associated with a block of 2048 data bits and may be used later to inhibit correlation of corrupted data. One complete frame of data is sent outside the chip into an external RAM and the following frame is put into a different RAM area, while the previously stored data are read out synchronously by a general clock common to the data streams coming from all other stations. This operation allows the realignment of data coming from different tapes.

Audio information reports time indication of the recorded data stream that is decoded by a small component. As in the previous case clock and data are

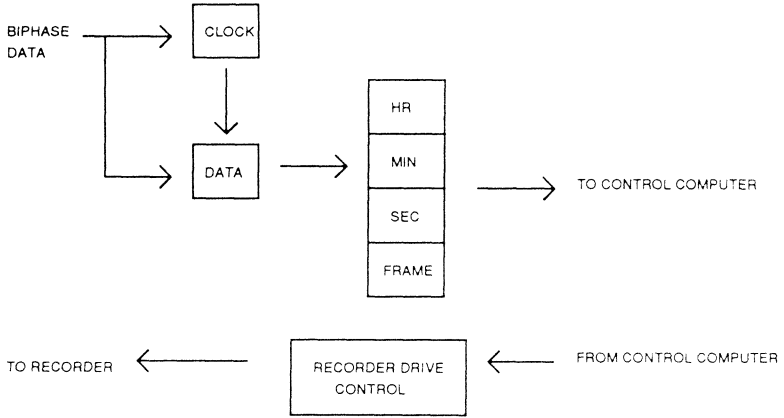


Fig. 4. Schematic view of the audio decoder chip.

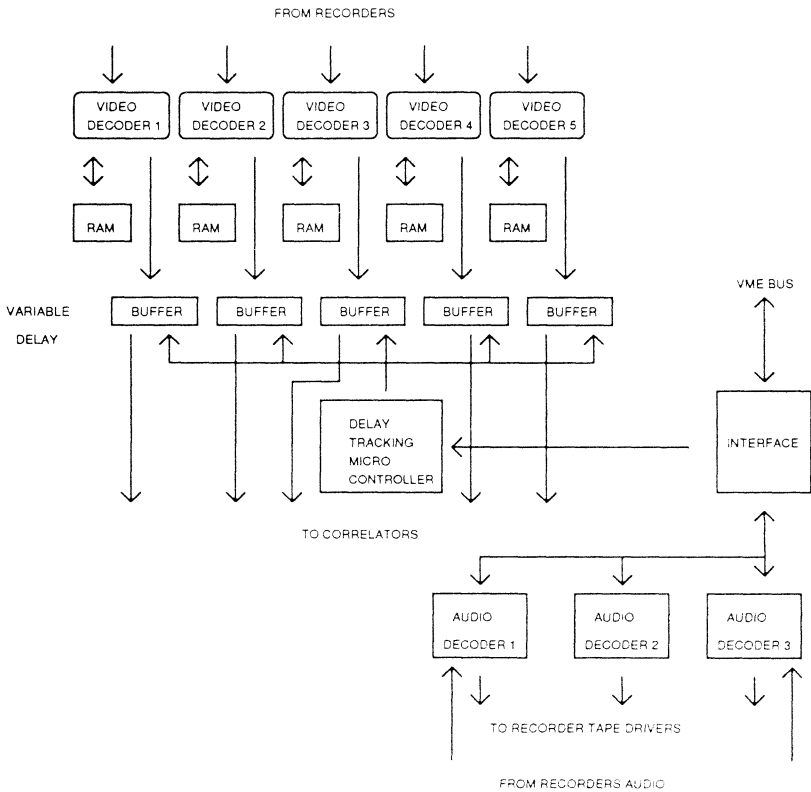


Fig. 5. Functional description for a board operating with 5 stations including data and time decoders and delay tracking control operating on VME bus.

reconstructed and the information of HR, MIN, SEC, FRAME number is BCD decoded (Fig. 4). Those data are available to external control in order to allow tape synchronisation within one frame resolution. The content of an internal register is used to drive the recorder.

Two complete audio decoders are contained in a 2000 gates equivalent device.

## 5. Overall View

A prototype of a complete 5 station correlator housing inside a VME environment is under development. One VME board contains 5 video and 5 audio (in 3 chips) decoders with the surrounding circuitry (Fig. 5). A microcontroller should be dedicated to delay tracking calculation and control. The board is responsible for data extraction, delay tracking and recorder control.

Two identical boards are able to support correlation of 5 stations (5 baselines each board) including rotators accomplished by a microcontroller for phase tracking (Fig. 6). The boxes indicated as C1 (A, B, ...) and C2 (A, B, ...) are the correlator + integrator chips, R (A, B, ...) represent the rotator chips. All three boards are computer controlled using a VME bus and a commercially available controller

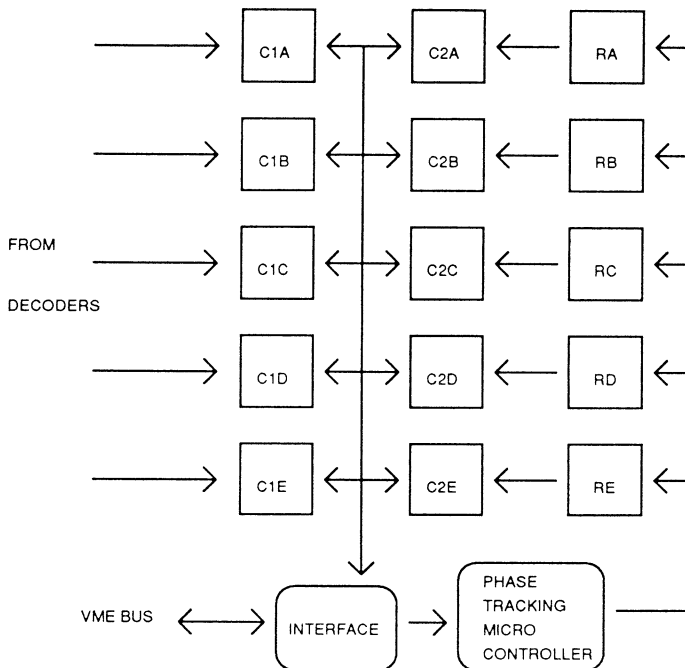


Fig. 6. Functional description for a board operating with 5 baselines with phase tracking control operating on VME bus.

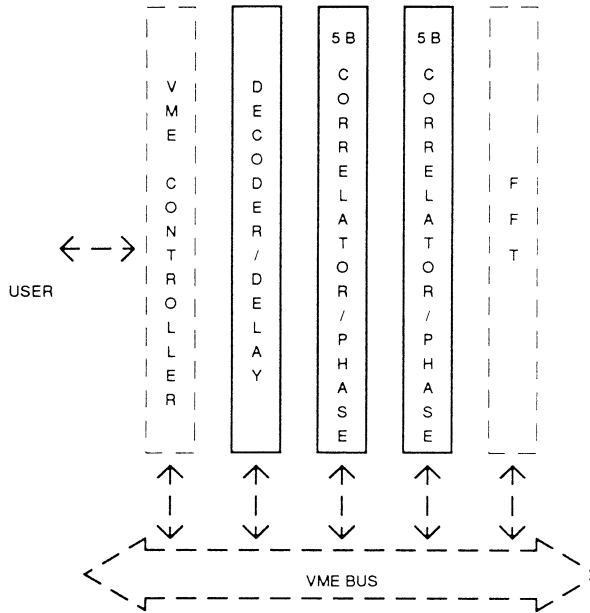


Fig. 7. Functional description for a system of 10 baselines operating on VME bus.

board. Figure 7 shows the general view of the correlator prototype. The user can retrieve data to process by FFT off line or the operation may be performed by the system itself by a dedicated DSP board.

The complete prototype features are:

- 5 stations with 8-16-32 lags;
- 4 stations with 12-24-48 lags;
- 3 stations with 24- 48-96 lags;
- 2 stations with 80-160-320 lags;
- maximum integration time 20'-1'-8 ms respectively at 4 MHz sample rate.

Components have been tested at 4 MHz but hopefully work with minor modifications at higher clock rates up to 16 MHz. Existing high speed components of the same FPGA family could be used to increase the maximum frequency of the system without redesigning needs.

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